HIL Evaluation of Power Flow Control Strategies for Energy Storage Connected to Smart Grid Under Unbalanced Conditions

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***Abstract*—This paper proposes two power flow control algorithms for a grid-connected voltage source converter used as part of the energy storage for a smart grid under unbalanced voltage conditions. Both algorithms are improvements of the dual vector current control algorithm (DVCC). The first proposed algorithm, DVCC_CL, optimizes the method of limiting phase currents for the duration of voltage unbalance. The second proposed algorithm, DVCC_HB, provides high bandwidth control of active and reactive power. Which of the two proposed algorithms is the better choice depends on the grid code requirements and the constraints imposed by the particular energy storage system which the inverter connects to the grid. The operation of both algorithms was verified within the framework of an ultralow-latency hardware-in-the-loop emulator, which makes accurate analysis of converter behavior safe and easy for any grid conditions.**

***Index Terms*—Current control, energy storage, hardware-in-the-loop (HIL), power control, power quality, smart grid.**

I. Introduction

THE need to integrate ever more renewable energy sources into the power grid requires ever more software to control and stabilize the grid at all levels. Such an intelligent grid is often called the smart grid [1]–[3].One of the key components of the smart grid is energy storage which is required to help stabilize grids having a high percentage of variable, noncontrollable energy sources such as wind or solar [4]–[6]. Inclusion of storage in the distributed generation system provides the network operators with the ability to stabilize the energy supply from its variable sources [7], [8]. There is a variety of technologies that can be used to store energy: ultracapacitors, flywheels, pumped hydro, fuel cells, batteries, etc. [7]. What all those technologies have in common is the need for a controllable power electronics (PEs) interface to the grid [9], [10]. This is most often realized in the form of a voltage source converter (VSC) as shown in Fig. 1.

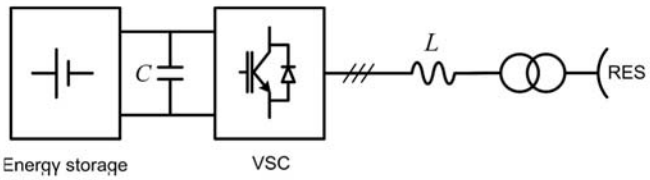

Fig. 1. VSC interface between an energy storage element and the "Smart grid."

One very important topic and the focus of this paper is the optimization of the control strategy for such a converter under unbalanced grid-voltage sags, which are quite common, particularly on weak grids. With a clever control strategy, such smart energy storage elements could play an important role in supporting the grid during faults by injecting optimal amounts of active and reactive power.

Voltage sags caused by network faults introduce negative-sequence grid voltage and current components. The control and operation of a grid-connected VSC under these circumstances have been widely investigated in the literature [11]–[22]. There are many grid codes which require grid support by active and reactive power injection during the fault in the event of voltage sags. However, specific requirements depend on the specific characteristics of each power system and the protection method employed. As a consequence of unbalanced conditions, oscillating components at twice grid frequency in both the active and reactive powers, as well as in the dc-link voltage, can appear [12], [13]. Song and Nam [12] proposed a dual-vector current controller (DVCC) to achieve robust operation of the VSC under generalized unbalanced input conditions. It is based on the separate regulation of positive and negative sequence components, allowing the delivery of a flattened active power to the grid, while suppressing oscillations at twice grid frequency and maintaining the desired average power factor. However, during severe voltage sags, there is no control over the line currents' magnitudes, so they could reach values several times higher than nominal. In order to overcome this undesirable effect, a modified DVCC with grid-current limitation [14] and output-power reduction [15] was proposed. The drawbacks of all these solutions are their inability to eliminate reactive power oscillations at twice grid frequency altogether with active power oscillations.

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Furthermore, all previous solutions required antiresonant or notch filters in closed control loops to obtain symmetrical components [11]–[15]. Antiresonant filter introduces nonrational transfer function as it leads to phase delay of the input signal [16]. A notch filter for this application usually has a second-order transfer function and can cause a large phase jump at the set frequency. Therefore, the use of these filters entails poor dynamic response, low controller bandwidth, and complicated controller-gain settings.

Suh and colleagues [16], [17] proposed a control strategy using dual current regulators with oscillating reference signals. They introduced a resonant-gain path to eliminate errors due to ac components. Similar techniques have been used in [18]–[26], but the problem with these approaches is the slow transient response at startup, especially in cases of severe voltage sags [27]. In addition, they are unable to simultaneously suppress oscillations in active and reactive power, which could be required in certain conditions.

This paper proposes two control schemes to solve power quality problems in energy storage-supported smart grids in cases of grid disturbances. The first one proposes an improvement in the calculation of the current references for a modified DVCC strategy with imposed current limitation. The second control scheme proposes an instantaneous active and reactive power control without filtering in the control loops. The advantages of the proposed control algorithms are high controller bandwidth and decoupled control of active and reactive power which, unlike the method in [14], exhibits no time-varying components. The side effect, however, is a nonsinusoidal grid-current waveform for the duration of unbalanced grid voltage.

A. Issue in Hardware-in-the-Loop Emulation of PEs Systems

Tests on energy storage-supported smart grids are difficult and costly to carry out on real systems due to the high power rating of the hardware, system complexity, difficulty associated with emulating grid disturbances, and the impracticability of disconnecting parts of a system for longer periods of time [28], [29]. The alternatives to final system testing are to either build a small-scale prototype [30], which is time consuming to setup, inflexible, labor intensive to use, and expensive, or to use hardware-in-the-loop (HIL) rapid prototyping simulation tools. HIL emulation refers to a system in which parts of a real system are replaced by a real-time emulation platform [31], [32]. A mathematical model representing the real hardware has to be detailed enough to truly represent any transients or faults in a real system. PE devices comprise a number of switches controlled on a small time scale. Switching behavior makes these circuits highly nonlinear. For these reasons, very tiny simulation time steps are required to reach acceptable levels of accuracy [33].

With conventional, off-the-shelf computers, it is very difficult to achieve small simulation time steps because solving methods are usually not optimized for PE applications and input/output (I/O) communication latencies are unacceptably high [34]–[36]. Only field-programmable gate-array (FPGA) technology can provide simultaneously the combination of ultralow latency (ULL) and massively paralleled processing

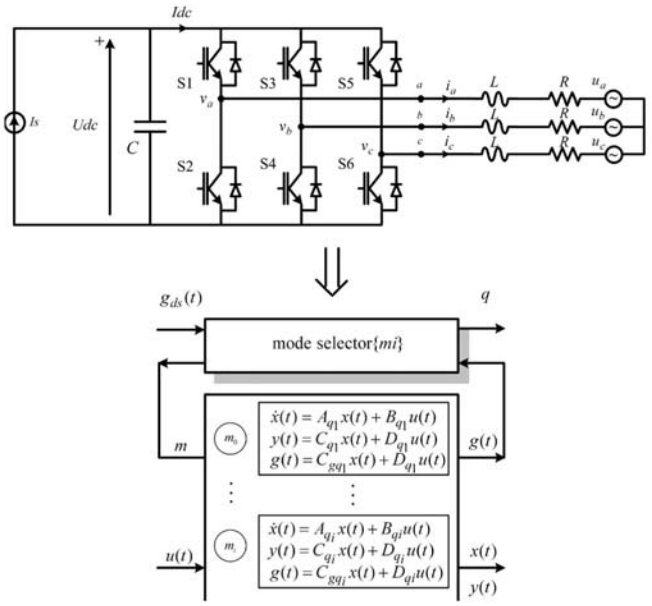

Fig. 2. PEs model abstraction.

required by a digital HIL emulator for PE designs [37]–[39]. An FPGA processor can be specifically tailored for the particular application to boost the performance of contemporary HIL simulators [40], [41]. However, the main problem is that developing simulation models on FPGAs requires extensive knowledge of digital design, computer architecture design, FPGA design and verification tool-chains, as well as a detailed understanding of PE modeling techniques. Still, the potential of FPGA technology has been recognized and solutions based on this technology are actively studied [42].

In this paper a universal, ULL HIL platform was used to evaluate the ability of the proposed algorithms to meet grid-code requirements in severely unbalanced grid conditions [43]. The entire hardware is emulated in real time on an FPGA platform with a fixed simulation time step of 1 μs. ULL enables high accuracy and much better transient response compared with other commercially available emulation platforms. The real-time simulator interacts with the controller via a low-latency I/O interface board. The control algorithm is realized using a control platform based on the TMS320F2812 DSP.

II. Hybrid Dynamic-System Modeling

PE systems are inherently nonlinear switched circuits where the control of power flow is achieved with precisely timed switching events [44]. The block diagram of a PE converter is shown in Fig. 2. The combination of continuous time dynamics (continuous-time state-space) and discrete events (finite automaton) that PE exhibits lends itself naturally to a hybrid system modeling approach. This motivated us to adopt the modeling framework based on generalized hybrid automaton (GHA) with piecewise linear continuous dynamics. PE circuits (grid-side inverter supported by energy storage) are represented with passive elements (R, L and C), piecewise linear switches, a controlled current source and independent voltage sources that yield

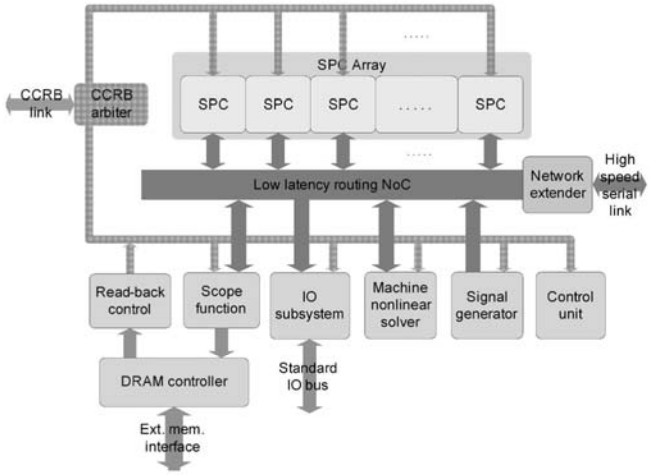

Fig. 3. Processor architecture.

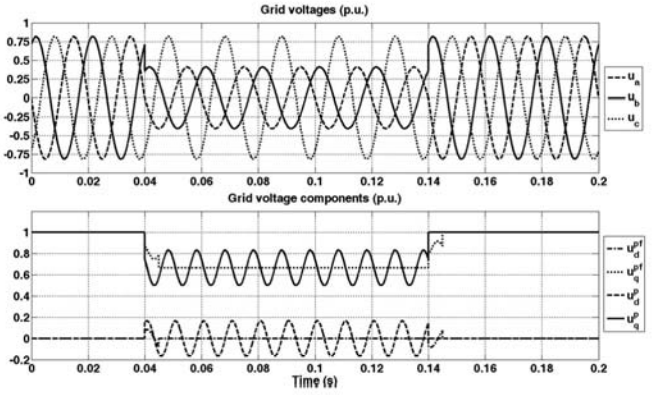

Fig. 4. Phase voltages in original and synchronously rotating reference frame.

a piecewise linear state-space representation, as shown in Fig. 2 and set of matrix (1) and (2)

$$\dot{x}(t) = A_{q_i}\dot{x}(t) + B_{q_i}u(t) \tag{1}$$

$$y(t) = C_{q_i}x(t) + D_{q_i}u(t) \tag{2}$$

where $x(t)$is the continuous state-space vector, $y(t)$is the output vector, and $u(t)$is the input vector. A_{q_i} and B_{q_i} are state-space matrices.

Any discrete state of the circuit belongs to a finite set $Q = \{q_1 \cdots q_m\}$ that further defines given the state-space representation. Every discrete state q_i, therefore, has a unique dynamic behavior that we call mode m_{q_i}. In addition, each discrete transition $e \in (q_i, q_k)$has an assigned vector of switching signals g. Since not all the discrete state-to-state transitions are possible, the collection of allowable discrete transitions is predefined [43].

A. *Computational Platform Tailored for the Hybrid System*

In order to take full advantage of the simulation approach, a computational platform was proposed that can compute GHA models in real time with predictable timing and good fidelity. The strict real-time requirements translate into the need for ultra-high speed, deterministic, and time-predictable model computation, memory management, and I/O communication latency.

In order to satisfy all of the aforementioned requirements, we developed a new processor architecture, illustrated in Fig. 3, and explained in detail in [43].

The digital processor comprises an array of standard processing cells (SPC) which can be thought of as GHA application-specific processor cores. Each SPC is fully programmable and solves a GHA submodel up to a parameterized level of complexity in terms of number of switches and number of passive storage elements. All SPC units operate synchronously and in parallel, each accessing its individual memory resources. The communication that is not latency critical, such as connection to the external PC, is implemented with a dedicated control, configuration, and read-back bus.

III. Mathematical Description of Voltage Source Inverter Under Unbalanced Grid Voltages

When grid disturbances, such as voltage sags, phase jumps, or amplitude variations occur, the system voltages and currents could be represented by their positive and negative sequence components. Therefore, an unbalanced system of the three phase voltages (u_a, u_b, u_c) could be represented with its positive $(u^p_{dq} = u^p_d + ju^p_q)$ and negative sequence $(u^n_{dq} = u^n_d + ju^n_q)$ components, as given by

$$u_{\alpha\beta} = e^{j\omega t}u^p_{dq} + e^{-j\omega t}u^n_{dq} \tag{3}$$

where $u_{\alpha\beta} = \sqrt{2/3}\left(u_a + u_b e^{j2\pi/3} + u_c e^{-j2\pi/3}\right)$ is the grid voltage vector expressed in the stationary reference frame (using a power-invariant transformation) and ω is the angular grid frequency. In the same manner, unbalanced grid currents also appear and they could be represented in terms of positive and negative sequence current components, similar to (3)

$$i_{\alpha\beta} = e^{j\omega t}i^p_{dq} + e^{-j\omega t}i^n_{dq} \tag{4}$$

where $(i^p_{dq} = i^p_d + ji^p_q)$ and $(i^n_{dq} = i^n_d + ji^n_q)$.

One case of unbalanced grid voltages in the original and synchronously rotating reference frame is shown in Fig. 4. It should be noted that in the positive sequence reference frame, a positive component appears as dc, whereas a negative component oscillates at twice the grid frequency. In the negative reference frame, it is the opposite, which is explained thoroughly in [12].

The representation of a two-level VSC, used as an interface in energy storage applications, could be described by differential (5) in the stationary reference frame

$$v_{\alpha\beta} = u_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} + Ri_{\alpha\beta} \tag{5}$$

where R is grid resistance, L is grid inductance and

$$v_{\alpha\beta} = \sqrt{\frac{2}{3}}\left(v_a + v_b e^{j2\pi/3} + v_c e^{-j2\pi/3}\right) \tag{6}$$

$$i_{\alpha\beta} = \sqrt{\frac{2}{3}}\left(i_a + i_b e^{j2\pi/3} + i_c e^{-j2\pi/3}\right) \tag{7}$$

where $v_{\alpha\beta}$ and $i_{\alpha\beta}$ denote the converter pole voltages and line currents, respectively.

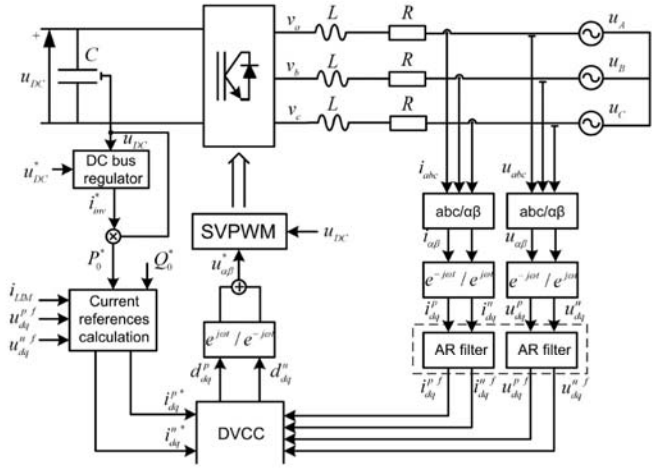

Fig. 5. VSC control using DVCC_CL.

Equation (5) can now be transformed and decomposed into two parts in the positive and negative synchronous rotating reference frames, respectively, as shown in the following equations [12]:

$$v_{dq}^{p} = L\frac{di_{dq}^{p}}{dt} + Ri_{dq}^{p} + j\omega Li_{dq}^{p} + u_{dq}^{p} \tag{8}$$

$$v_{dq}^{n} = L\frac{di_{dq}^{n}}{dt} + Ri_{dq}^{n} - j\omega Li_{dq}^{n} + u_{dq}^{n}. \tag{9}$$

With regard to this, instantaneous apparent power could be expressed as

$$s = u_{\alpha\beta}i_{\alpha\beta}^{*} = p(t) + jq(t) \tag{10}$$

where active power $p(t)$ and reactive power $q(t)$ are

$$p(t) = P_0 + P_{c2}\cos(2\omega t) + P_{s2}\sin(2\omega t) \tag{11}$$

$$q(t) = Q_0 + Q_{c2}\cos(2\omega t) + Q_{s2}\sin(2\omega t). \tag{12}$$

Terms P_0 and Q_0 designate the value of the average power, whileP_{c2}, P_{s2}, Q_{c2}, and Q_{s2} are the magnitudes of the power oscillations caused by the unbalance. Detailed expressions for all six terms are given in [12].

IV. Modified DVCC With Current Limitation

Song and Nam recommended the DVCC to achieve robust operation of a VSC under unbalanced grid-voltage conditions [12]. Its core is the regulation of positive and negative sequence components, allowing the transfer of active power to the grid at grid frequency, while suppressing the oscillations at twice grid frequency and maintaining the desired average power factor.

A conventional DVCC cannot be implemented under extreme voltage conditions [17]. For severe voltage sags, grid currents could reach unacceptably high values, several times higher than the nominal value. For reliability and converter protection reasons, this should not be permitted. Therefore, the modified DVCC with imposed current limitation (DVCC_CL) is recommended [14]. The control structure of such an improved system is shown in Fig. 5.

The three-phase grid voltages and currents are measured and transformed into a stationary ($\alpha\beta$) and a synchronously rotating reference frame *dq*. As in a conventional DVCC, it is necessary to regulate both positive and negative sequence components, which are obtained by applying the transformation of rotation in both directions. Due to the fact that a conventional DVCC operates with dc signals only, an antiresonant filter is used in order to extract the sequence components [14], [24]. Likewise, the filtered *dq* components of voltage are needed in the current reference calculation block.

The current controller (DVCC) used here consists of a pair of PI controllers that control the positive and negative sequence components separately and are implemented in two different rotating reference frames. Details about the controllers and the extraction of sequence components can be found in [12] and [14].

In order to generate the proper current references, we should consider the following equation:

$$\begin{bmatrix} I_{\mathrm{GRID}}^{2} \\ Q_0 \\ P_{C2} \\ P_{S2} \end{bmatrix} = \begin{bmatrix} I_{\mathrm{LIM}}^{2} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} i_d^{pf*} & i_q^{pf*} & i_d^{nf*} & i_q^{nf*} \\ u_q^{pf} & -u_d^{pf} & u_q^{nf} & -u_d^{nf} \\ u_q^{nf} & -u_d^{nf} & -u_q^{pf} & u_d^{pf} \\ u_d^{nf} & u_q^{nf} & u_d^{pf} & u_q^{pf} \end{bmatrix} \times \begin{bmatrix} i_d^{pf*} \\ i_q^{pf*} \\ i_d^{nf*} \\ i_d^{nf*} \end{bmatrix}. \tag{13}$$

The superscript *f* indicates that the quantities are filtered. The first condition in a conventional DVCC concerns the desired power flow $P_0 = P_0^{*}$, but this is now replaced by the current limiting condition, $I_{\mathrm{GRID}}^{2} = I_{\mathrm{LIM}}^{2}$, while the actual active power is determined by grid voltages and the set current limit. Solving (13), the current references are obtained as

$$i_d^{pf*} = \frac{I_{\mathrm{LIM}}u_d^{pf}}{D} \tag{14}$$

$$i_q^{pf*} = \frac{I_{\mathrm{LIM}}u_q^{pf}}{D} \tag{15}$$

$$i_d^{nf*} = \frac{-I_{\mathrm{LIM}}u_d^{nf}}{D} \tag{16}$$

$$i_q^{nf*} = \frac{-I_{\mathrm{LIM}}u_q^{nf}}{D} \tag{17}$$

where $D = \sqrt{(u_d^{pf})^2 + (u_q^{pf})^2 + (u_d^{nf})^2 + (u_q^{nf})^2}$.

The power delivered from the energy storage to the grid is now smaller due to the decreased grid voltages and limited line currents.

Using this control structure, it is possible to eliminate dc-link voltage oscillations, as well as oscillations in active power. Unfortunately, with the current choice as in (13), it is not possible to eliminate oscillations in reactive power. On top of everything, this implies that an alternating reactive power exists

(time-varying component at twice grid frequency), although the average reactive power is equal to zero, or to another set value (Q_0).

Each coefficient in (13) corresponds to purely sinusoidal term in the stationary reference frame. When they are summed, the result is purely sinusoidal grid currents.

V. High-Bandwidth Power Flow Control Algorithm

In the DVCC_CL method, the set of (13) is not complete since reactive power oscillations (Q_{c2} and Q_{s2}) are not taken into account. The degrees of control freedom of the control, limited to i_d^{pf*},i_q^{pf*},i_d^{nf*}, and i_q^{nf*}, prevent any other way of annulling Q_{c2} and Q_{s2}.

In this section, we propose current references calculation based on instantaneous active and reactive power in the stationary reference frame, which allow simultaneous time-invariable active and reactive power control. In contrast to the previous control method, where the system currents were always sinusoidal, this method leads to nonsinusoidal currents.

The control strategy is based on a high-bandwidth dual-vector PI-based current controller with oscillating reference signals (DVCC_HB). The proposed control structure is similar to the one shown in Fig 5. The main difference is the absence of filters for obtaining symmetrical components in the control loops (marked with a dashed line in Fig. 5). The current reference calculation block is also different and will be explained later. There is no need for an antiresonant filter, as the newly proposed controller operates with the sum of dc and variable ac components, which are the result of unbalance. The dc-link voltage controller provides the proper power reference which is the input to the current-reference calculation block.

In order to achieve the desired active and reactive power flow control, it is necessary to calculate the appropriate current references. Expressions for active and reactive power could be given as in [45]

$$p(t) = u_\alpha i_\alpha + u_\beta i_\beta \tag{18}$$

$$q(t) = u_\beta i_\alpha - u_\alpha i_\beta. \tag{19}$$

If we supply references for active and reactive power together with grid voltages in the $\alpha\beta$ domain, grid-current references, combining the previous two equations, could be obtained as in [46]

$$i_\alpha^* = \frac{p^* u_\alpha + q^* u_\beta}{u_\alpha^2 + u_\beta^2} \tag{20}$$

$$i_\beta^* = \frac{p^* u_\beta - q^* u_\alpha}{u_\alpha^2 + u_\beta^2}. \tag{21}$$

When a voltage disturbance is sensed, current limitation is achieved by the proper setting of the active power reference

$$p^* = u_{\mathrm{dc}} I_{\mathrm{dcLIM}} \tag{22}$$

where $u_{dc}$is the dc-link voltage and $I_{\mathrm{dcLIM}}$is the current limit. References i_α^* and $i_\beta^*$are transformed into the *dq* reference frame and supplied to the DVCC_HB (see Fig. 6).

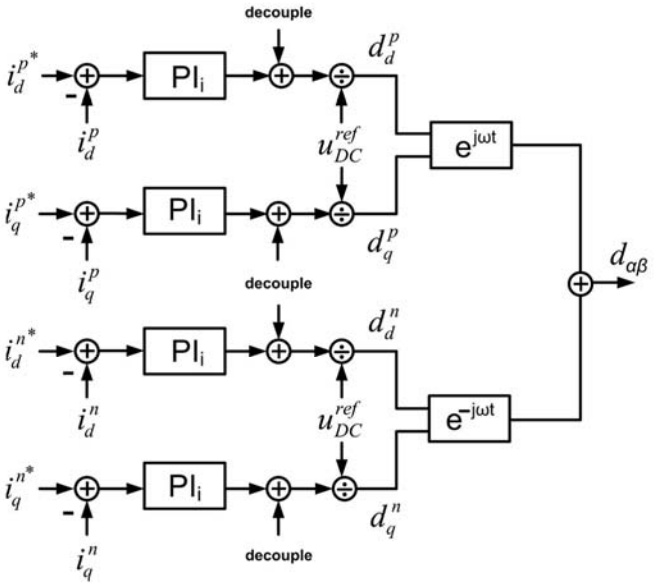

Fig. 6. DVCC_HB. Input currents are ac values.

The DVCC_HB consists of two decoupled controllers, one for the positive sequence component (two PI regulators for *d*- and *q*-axis, respectively) and one for the negative sequence component (two PI regulators for *d*- and *q*–axis, respectively). According to (3) and Fig. 4, there are dc and ac components at the input of each controller (no filter is used). Fig. 7 shows that the dc component from the input of the PI controller i_d^p (dashed line signal) appears as an ac component at the input of the lower PI controller (solid line signal). The dc component from the input of the lower PI controller i_d^n appears as the ac component at the input of the upper PI controller. Although one PI controller, by itself, cannot track an ac reference without a steady-state error, each of the PI controllers will bring the corresponding dc component to its reference value (for example, i_d^p to i_d^{p*}). Combination of their influence in positive and negative reference frames will lead to automatically tuned both dc and ac components to their desired values.

The main advantage of the proposed solution lies in avoiding filters for obtaining the symmetrical components needed in closed control loops. Such an approach provides high control loop bandwidth, increases the system stability margin, and simplifies controller gain settings.

VI. Controller Settings

A. DVCCs

In previous work, the design of DVCCs has proven to be quite challenging due to the antiresonant filter used in the feedback control loops. The consequence of using such a conventional filter is the time delay it causes, resulting in poor transient response. Apart from this, it includes a transfer function which could lead to the phase lag of a control signal.

As explained in the previous section, in the case of the DVCC_HB algorithm, we used conventional PI regulators. The system dynamics are represented by (8) and (9). By solving

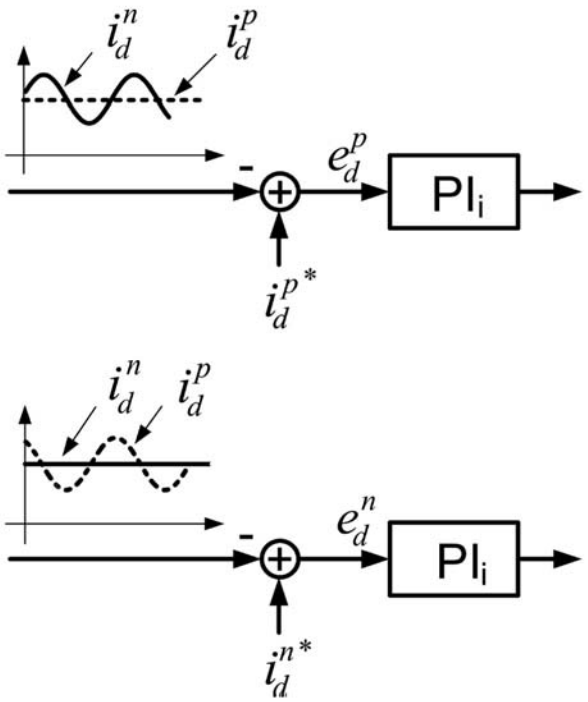

Fig. 7. Operation principle of DVCC_HL.

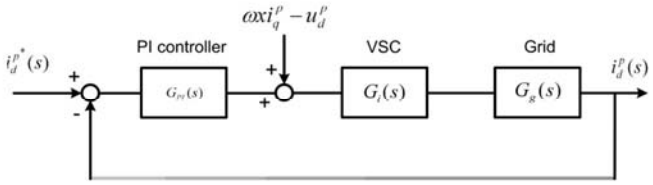

Fig. 8. Current controller parameter settings.

them, the controller gains could easily be obtained. For example, the control loop for i_d^p current can be represented as shown in Fig. 8 containing a PI controller, VSC, and grid transfer function. The term $\omega x i_q^p - u_d^p$, where x is the grid reactance expressed in p.u., is inserted to decouple the *dq* axes dynamically.

The corresponding open loop transfer function is given as follows:

$$G_{OL}(s) = G_{\mathrm{PI}}(s)G_i(s)G_g(s) = \left(K_{Pi}\frac{\tau_{\mathrm{PI}}s+1}{\tau_{\mathrm{PI}}s}\right)\left(\frac{1}{(T_s/2)s+1}\right)\left(\frac{1/r}{(L/R)s+1}\right) \tag{23}$$

where $r = R/Z_B$ is the grid resistance expressed in p.u., L is the grid inductance in absolute values, and T_s is the switching period. We chose to determine regulator parameters based on the symmetrical criterion [47]. According to this criterion, time constant τ_{PIi} from (23) needs to be set to $\tau_{PIi} = 4(T_s/2) = 2T_s$. Now the proportional and integral gains are obtained as

$$K_{Pi} = \frac{L}{2Z_B T_s} \tag{24}$$

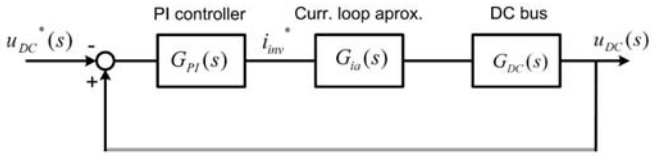

Fig. 9. DC-link voltage controller parameters settings.

$$K_{Ii} = \frac{K_{Pi}}{\tau_{\mathrm{PI}i}} = \frac{L}{4Z_B T_s^2}. \tag{25}$$

For practical implementation, the controller is transformed into a time-discrete form using bilinear transformation.

B. DC-Link Voltage Controller

DC-link voltage control ensures correct transfer of the power from the energy storage to the grid. DC link and the energy storage can be modeled as a capacitor with a current source in parallel. This control loop implements a simple PI controller, which outputs the reference for the inverter dc current (i_{inv}^*). The control structure of the dc voltage regulator is described in Fig. 9.

The open-loop transfer function of dc-link regulator is given as

$$G_{\mathrm{OL}}(s) = G_{\mathrm{PI}}(s)G_{ia}(s)G_{\mathrm{DC}}(s) = \left(K_{\mathrm{Pdc}}\frac{\tau_{\mathrm{PIdc}}s+1}{\tau_{\mathrm{PIdc}}s}\right)\left(\frac{1}{(T_u/2)s+1}\right)\left(\frac{1/(C\cdot Z_B)}{s}\right). \tag{26}$$

The current control loop is here approximated by a first-order delay block and it is assumed that its dynamics is an order of magnitude faster than the dc-link control-loop dynamics.

The symmetrical criterion can also be applied to the dc-link controller setup

$$K_{Pdc} = \frac{CZ_B}{2T_u} \tag{27}$$

$$K_{Idc} = \frac{K_{Pdc}}{\tau_{PIdc}} = \frac{CZ_B}{4T_u^2} \tag{28}$$

where T_u is the sampling period of the loop and should be set to $T_u = 8T_s$.

VII. Simulation Results

In order to verify the control principles proposed in this paper, first a detailed model of the system was developed in MATLAB/Simulink. The system data are shown in Table I. Simulations were carried out for both control structures: DVCC_CL and DVCC_HB. The results are compared in detail. The simulation results shown in Figs. 10 and 11 illustrate the performance of a grid-connected inverter used in an energy storage application with the proposed DVCC_CL used to deal with unbalance. It is supposed that voltage dips start at about 40 ms and have a duration of 100 ms. It is a sag Type B (one phase drop, in this case, Phase b) [48] with a remaining voltage of 40%.

TABLE I
SYSTEM DATA

Quantity	Symbol	Value	Value in p.u.
Nominal AC voltage	U_n	6 kV	1
Nominal frequency	f_n	50 Hz	
Nominal DC voltage	U_{DC}	10.8 kV	1.8 (dc)
DC link capacitance	C	2 mF	
Grid resistance	R	0.1 Ω	0.0064
Grid reactance	L	4 mH	0.08
Base impedance	Z_B	15.8Ω	1
Switching frequency	f_s	2 kHz	
Switching period	T_s	500 μs	

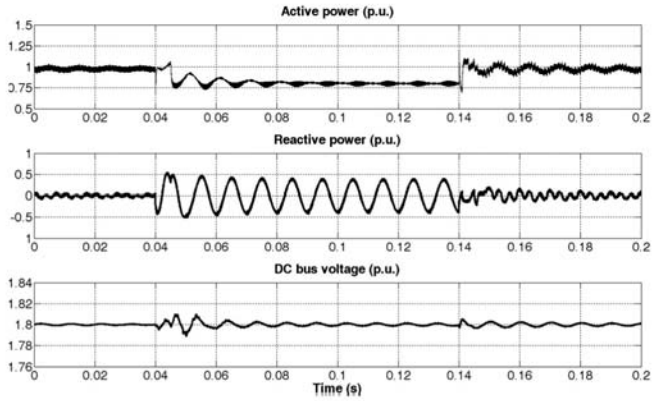

Fig. 10. Active power, reactive power, and dc-link voltage response with DVCC_CL.

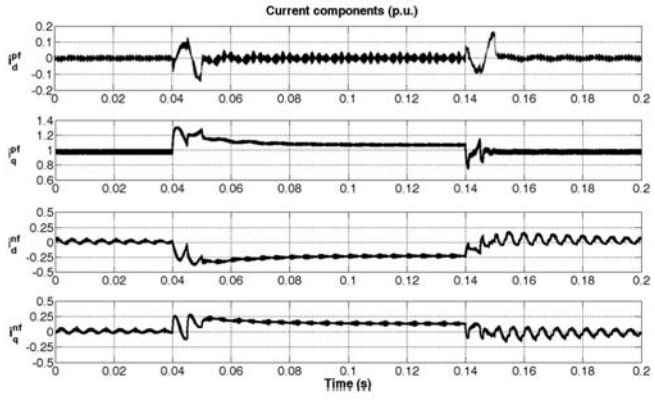

Fig. 11. Grid current components' response with DVCC_CL.

It could be observed that the DVCC_CL can eliminate active power oscillations during unbalanced grid-voltage conditions. However, it is not possible to eliminate oscillations at twice the grid frequency in the reactive power, which is in accordance with the explained control method. During the disturbance, the DVCC_CL effectively limits the magnitude of the grid current to $I_{LIM} = 1.1(p.u.)$. Current limit can vary depending on the type of voltage sag and the current capability of the VSC. This is explained in detail in [15]. A lower grid voltage and a limited grid current imply a decrease in active power flow from the energy storage to the grid. The stable dc-link voltage indicates that the power transfer is correctly managed. The grid-current component response is shown in Fig. 11. It can be seen that they

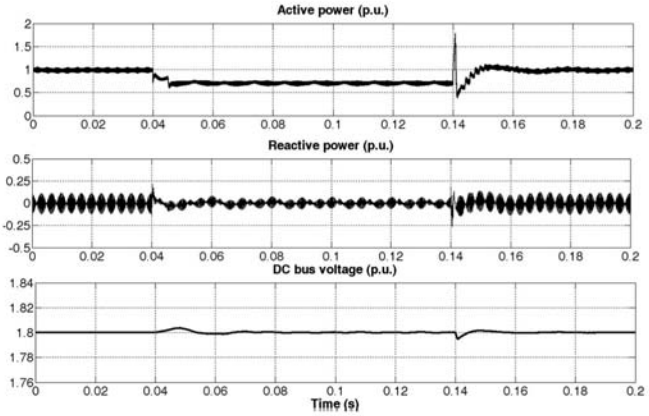

Fig. 12. Active power, reactive power, and dc-link voltage response with DVCC_HB.

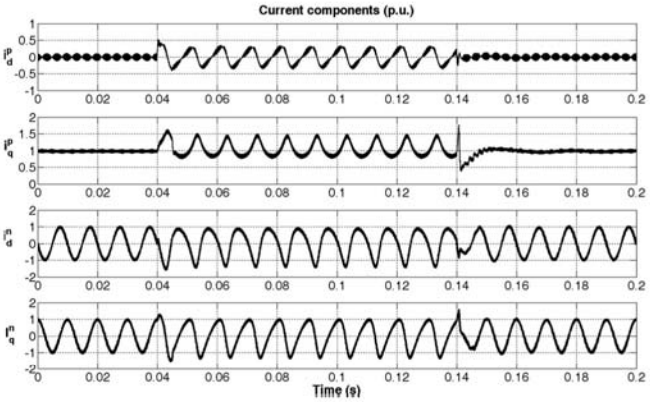

Fig. 13. Grid current components' response with DVCC_HB.

are dc values, which is due to the antiresonant filter employed in the feedback control loops.

The simulation results given in Figs. 12 and 13 show the DVCC_HB controller response to an unbalanced voltage sag when two of the phases have magnitudes of 50% of nominal. It should be noted that there are neither active nor reactive power oscillations during the voltage sag, in accordance with the predefined aims. The proposed control structure is also an effective way of limiting the grid current and maintaining a stable dc-link voltage. The active power is lower due to the current limitation. Fig. 13 illustrates the current components' response. It can be concluded that the current components are not sinusoidal, which is a consequence of the constant active and reactive power control. During the voltage sag, it is impossible to achieve both reactive power equal to zero and sinusoidal current waveforms, but this control structure could be used when flattened active and reactive power is required.

VIII. SYSTEM PERFORMANCE VERIFICATION USING HIL

A. HIL Emulation

In this paper, a universal ULL HIL FPGA-based platform, dedicated to PEs applications, is used [43]. The proposed platform comprises the emulator hardware and application software that supports a variety of circuit configurations. The parameters

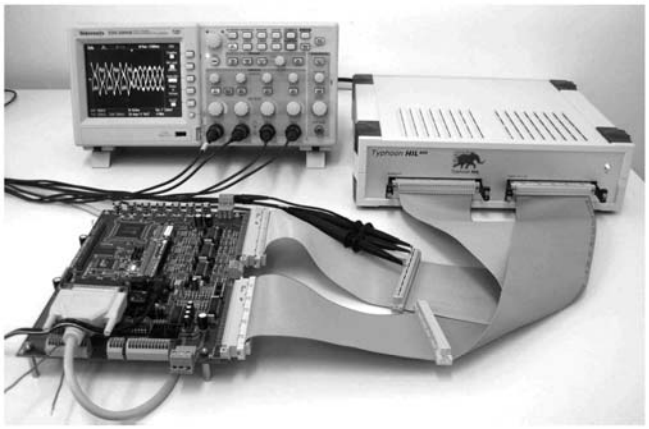

Fig. 14. Hardware setup. HIL platform is on the right. TMS320F281 DSP control board is on the left.

of the circuit could be easily modified by means of a circuit compiler. The circuit compiler consists of a schematic editor to describe the PE circuit to be simulated in real time and software that compiles the circuit description into instructions for the processor. An intuitive graphical user interface allows the user to set up the HIL simulation parameters, select control variables and variables to be displayed, run and stop the emulation, set up signal offsets, and change model parameters online.

B. Real-Time Implementation

The system hardware is simulated in real time on the HIL platform with a time step of 1 μs, since the pulsewidth modulation (PWM) carrier frequency is 2000 Hz. The models of the PWM inverter, dc link, and grid are simulated using an HIL 400 emulator [43]. Control algorithms are realized using a control platform based on the TMS320F2812 DSP [49]. In each switching period, the DSP has to complete the following tasks:

1) measure the grid voltages and currents as well as the dc-link voltage;
2) perform analog to digital conversion of the measured data;
3) determine grid electrical angle using PLL robust to grid distortion;
4) detect voltage sag;
5) calculate positive and negative sequence voltages and currents (with or without antiresonant filter, depending on control strategy);
6) calculate current references (DVCC_CL or DVCC_HB) using (13), (20), and (21);
7) execute controller functions (see Fig. 6);
8) implement dc-link control; and
9) generate the SVPWM voltage and feed it to the simulator digital inputs.

The hardware and setup are shown in Fig. 14. On the right side, we can see the HIL emulator box and on the left side we can see the DSP-based controller.

The general hardware architecture of the HIL 400 emulator is shown in Fig. 15. A Xilinx FPGA Virtex 5 board is the core of the HIL platform. Communication between the FPGA board and the PC is achieved through an Ethernet link, while signals needed for ezDSP TMS320F2812 controller are exchanged thorough the custom made low-latency I/O board. It provides 8 analog inputs, 16 analog outputs (AO), 32 digital inputs (DI), and 32 digital outputs. AO are used to transfer feedback signals (grid currents and voltages and dc-link voltage) to the controller and for measurement. PWM control signals are transferred from the ezDSP to the HIL platform through the DI control unit. In this way currents and voltage control loops are established.

C. HIL Experimental Results

In this section, the performance of the proposed HIL controller was verified comparing it with the simulation results shown in the previous section. Experimental results shown in Figs. 16 and 17 illustrate the performance of the DVCC_CL controller. The voltage sag is the same as simulated in MATLAB (Type B sag, one phase drop with a remaining voltage of 40%). An excellent match between simulation and HIL emulation was observed. In the steady state, the values of active and reactive power, dc-link voltages and currents are all the same as in the MATLAB/Simulink simulation. Transient responses have a similar shape but there is a slight difference caused by imperfect voltage-sag detection in the real hardware (it is impossible to detect it instantaneously) and the antiresonant filter which introduces a time delay of 5 ms and degrades the transient response.

Grid currents in the original domain are shown in Fig. 18. It can be seen that during the voltage sag, currents are unbalanced but sinusoidal. Currents are limited because of the converter protection strategy.

The DVCC_HB controller performance is described in Figs. 19 and 20. The two-phase voltage sag to 50%, as in the previous section, is employed. In this case, the transient response is improved since there is no antiresonant filter in the control loop. If we compare these diagrams with those in Figs. 10 and 11, we see a good match.

Grid currents in the original domain are shown in Fig. 21. It can be seen that during the voltage sag, currents are unbalanced and distorted. Currents are limited by the converter protection strategy.

The detailed explanations and conclusions for the diagrams obtained in Section VI are valid here also.

In order to further understand the difference between the two proposed DVCC control methods, the results of the current-harmonic analyses will be compared. The spectral content of one phase current during the voltage sag for DVCC_CL and DVCC_HB are shown in Figs. 22 and 23, respectively. Results are compared with the off-line simulation. In both cases, results are normalized comparing them with the first-order harmonic which is 100%. Total harmonic distortion (THD) for every case is also given.

The harmonic spectrum for the DVCC_CL control method (see Fig. 22) corresponds to sinusoidal grid current waveform where, apart from the first harmonic, high-order harmonics located around the PWM switching frequency (2000 Hz) and their multiples appear. Low-order harmonics are canceled due to the selected control method.

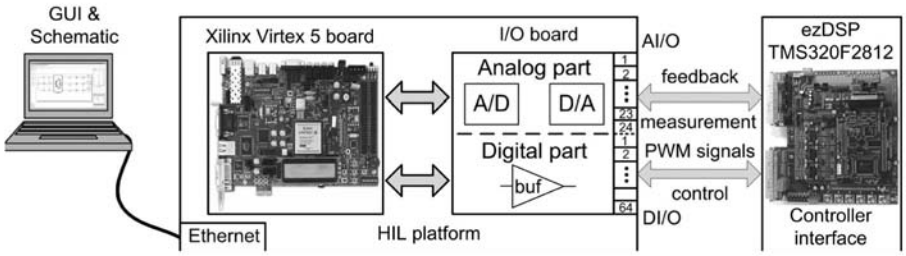

Fig. 15. HIL emulator hardware description.

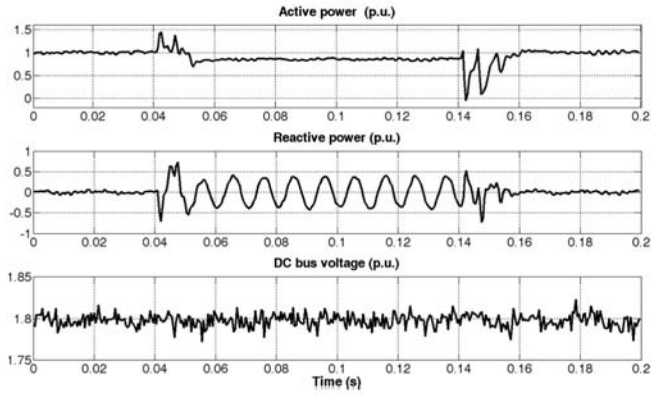

Fig. 16. Active power, reactive power, and dc-link voltage response. DVCC_CL_HIL experimental results.

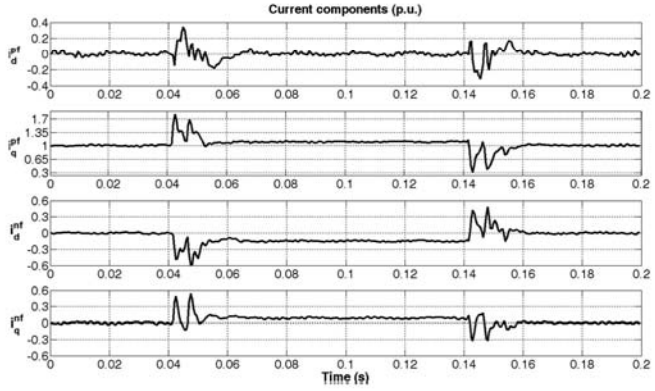

Fig. 17. Grid current components' response. DVCC_CL_HIL experimental results.

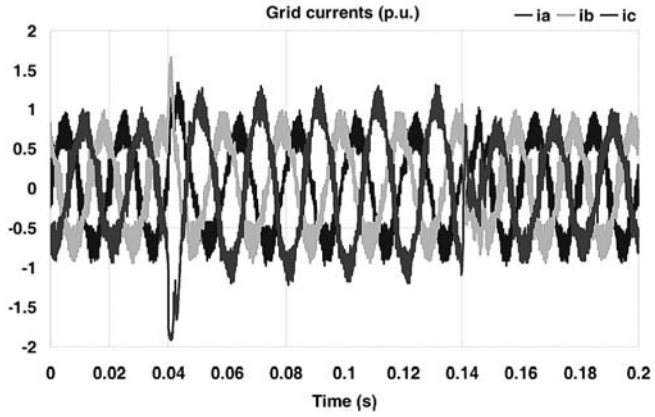

Fig. 18. Grid currents in original domain. DVCC_CL_HIL experimental results.

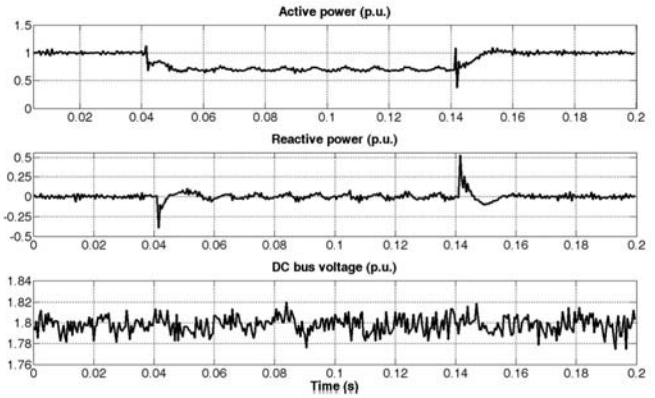

Fig. 19. Active power, reactive power and dc-link voltage response. DVCC_HB_HIL experimental results.

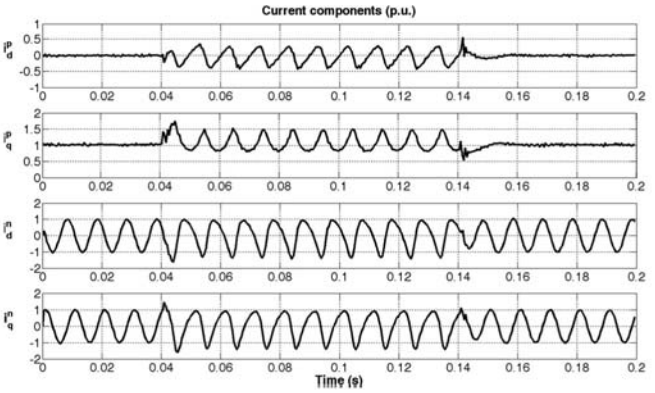

Fig. 20. Grid current components' response. DVCC_HB_HIL experimental results.

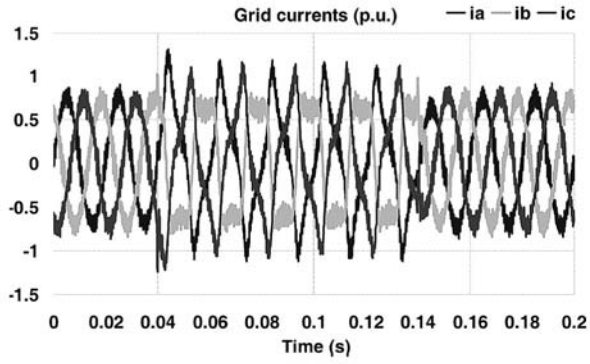

Fig. 21 Grid currents in original domain. High DVCC_HB_HIL experimental results.

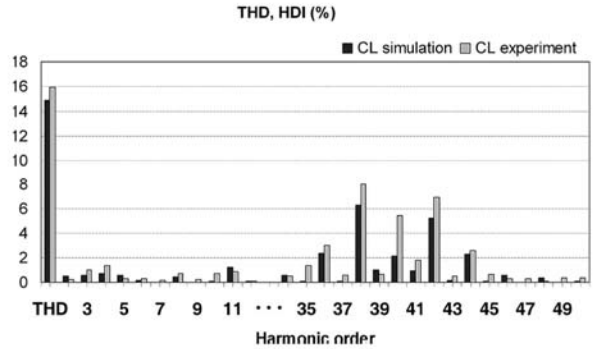

Fig. 22. Spectra of i_a current (the worst case) and current THD. DVCC_CL_HIL experimental results.

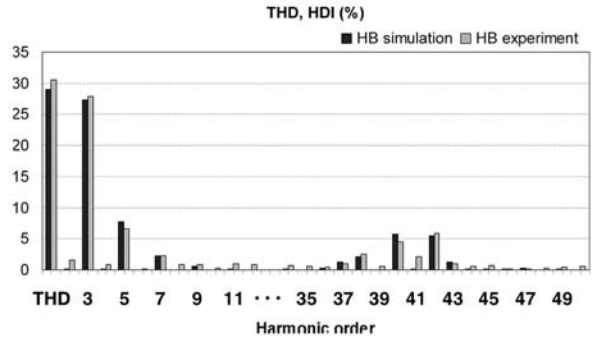

Fig. 23. Spectra of i_a current (the worst case) and current THD. DVCC_HB_HIL experimental results.

Unlike the previous control method, in the DVCC_HB controller, unbalanced voltage sag and requirements for time-invariable active and reactive power lead to nonsinusoidal grid currents. The harmonic spectrum is shown in Fig. 23. Low-order harmonics (third, fifth, etc.) are present which leads to greater overall THD. Harmonics between 14th and 34th are not shown because their influence is negligible. Simulation and HIL results are well matched.

IX. Conclusion

This paper proposed two novel power flow control strategies for energy storage systems connected to a smart grid under unbalanced conditions. The algorithms were implemented on a TMS320F2812 DSP and their performance is verified by means of an HIL emulator.

Both methods bring noticeable performance improvements over solutions proposed in the literature. The DVCC_CL method introduces the possibility of limiting the inverter current in a new way under unbalanced conditions, while the DVCC_HB method introduces the simpler controller structure (which does not need a filter to extract symmetrical components) and a higher bandwidth control loop.

For the duration of voltage unbalance conditions, the DVCC_CL algorithm produces constant active power, sinusoidal phase currents albeit with oscillating reactive power, while the DVCC_HB has a nonoscillating active and reactive power and high-bandwidth control but nonsinusoidal currents.

Which of the two algorithms is better suited for actual implementation depends on the grid code requirements that are, in turn, not yet fully explicit for an unbalanced grid and also on the specific constraints imposed by the actual energy storage method.

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